CLAIMS

What is claimed:

1. A method, comprising:

a) taking the absolute difference of:

1) less than all of the bits of an uncompressed video data value from a reference macro block;

2) less than all of the bits of an uncompressed video data value from a macro block worth of data within a search window;

b) calculating a sum of absolute differences between corresponding data values within said reference macro block and said macro block worth of data, said absolute difference being one of said absolute differences; and,

c) calculating a motion vector based upon the position of said reference macro block in a first frame and the position of said macro block worth of data in said second frame, said sum of absolute differences being a lowest sum of absolute amongst other sums of absolute differences calculated between said reference macro block and other macro blocks worth of data within said search window.

2. The method of claim 1 wherein said first frame is a current frame and said second frame is previous frame.

3. The method of claim 1 further comprising loading said reference macro block's data values into a register prior to said taking.

4. The method of claim 1 wherein said reference marco block's data values are uncompressed when said loaded.

5. The method of claim 3 further comprising loading said search wndow 's data values into a random access memory prior to said taking.

6. The method of claim 5 wherein said reference marco block's data values are uncompressed when said loaded ad said search window's data values are uncompressed when said loaded,

7. The method of claim 1 further comprising determining which N bits from:

1) said reference macro block's data value's M bits

2) said search window macro block's data value's M bits

are to be used for said taking the absolute difference.

8. The method of claim 7 wherein said determining comprises:

determining the number of most significant bits that are to be masked from both said data values;

determining the number of least significant bits that are to be masked from both said data values.

9. The method of claim 8 wherein said determining the number of least significant bits is (N-M) – (said determined number of mot significant bits).

10. The method of claim 9 wherein said determining the number of most significant bits further comprises calculating $\log_2|2^M/\text{MaxValue}|$ were MaxValue is the maximum uncompressed video data value of said reference macro block.

11. The method of claim 9 further comprising adding an offset value to said reference macro block's uncompressed video data value and said search window macro block's uncompressed video data value.

12. The method of claim 11 wherein said offset is set equal to a minimum valued uncompressed video data value of said reference macro block.

13. An apparatus, comprising:

a) logic circuitry to take an absolute difference between:

1) less than all of the bits of an uncompressed video data value from a reference macro block;

2) less than all of the bits of an uncompressed video data value from a macro block worth of data within a search window;

b) a register to store said reference macro block, said register coupled to said logic circuitry; and,

c) a random access memory to store said search window, said random access memory coupled to said logic circuitry.

14. The apparatus of claim 13 further comprising additional logic circuitry to determine an offset to be added to:

1) said reference macro block's uncompressed video data value; and,

2) said search window macro block's uncompressed video data value.

15. The apparatus of claim 14 further comprising a first adder having a first input to receive said reference macro block's uncompressed video data value and a second input coupled to said additional circuitry to receive said offset, said adder having an output that flows toward said logic circuitry.

16. The apparatus of claim 14 further comprising a second adder having a first input to receive said search window macro block's uncompressed video data value and a second input coupled to said additional circuitry to receive said offset, said adder having an output that flows toward said logic circuitry.

17. The apparatus of claim 13 wherein said logic circuitry is also to:

determine the number of most significant bits that are to be masked from both said data values;

determine the number of least significant bits that are to be masked from both said data values.

18. An apparatus, comprising:

a) logic circuitry to take an absolute difference between:

1) less than all of the bits of an uncompressed video data value from a reference macro block;

2) less than all of the bits of an uncompressed video data value from a macro block worth of data within a search window;

b) a register to store said reference macro block, said register coupled to said logic circuitry;

c) a random access memory to store said search window, said random access memory coupled to said logic circuitry; and,

d) a DRAM memory coupled to said register and said random access memory, said DRAM memory to store said uncompressed video data value from a reference macro block and said uncompressed video data value from a macro block worth of data within a search window

19. The apparatus of claim 18 further comprising additional logic circuitry to determine an offset to be added to:

1) said reference macro block's uncompressed video data value; and,

2) said search window macro block's uncompressed video data value.

20. The apparatus of claim 15 further comprising a first adder having a first input to receive said reference macro block's uncompressed video data value and a second input coupled to said additional circuitry to receive said offset, said adder having an output that flows toward said logic circuitry.

21. The apparatus of claim 19 further comprising a second adder having a first input to receive said search window macro block's uncompressed video data value and a second input coupled to said additional circuitry to receive said offset, said adder having an output that flows toward said logic circuitry.

22. The apparatus of claim 18 wherein said logic circuitry is also to:

determine the number of most significant bits that are to be masked from both said data values;

determine the number of least significant bits that are to be masked from both said data values.